REMARKS

Initially, Applicant acknowledges, with appreciation, Examiner Ho's courtesy of sending a new Form PTO-892 to Applicant on April 7, 2004.

At the time of the Office Action dated January 14, 2004, claims 1-20 were pending. Applicant acknowledges, with appreciation, the Examiner's indication that claims 7 and 14 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 1-6, 8-13 and 15-20 stand rejected.

In this Amendment, claims 2, 5-9, 12-14 and 20 have been amended only for better form. Care has been exercised to avoid the introduction of new matter.

The Examiner requested correction of errors in the specification. Applicant has made cursory review of the specification, but did not find typos or grammar errors in the specification.

Claim Objections.

Claims 5-7, 8, 12-14 and 20 have been objected to because of informalities. With respect to claims 5 and 12, the Examiner suggested to revise the recitation of "a third logic circuit" or the dependency of the claims. In response, Applicant has revised the recitation to --a second logic circuit--, as attached. Applicant has also amended claims 6-8, 13, 14 and 20 in a manner consistent with the Examiner's suggestions, i.e., changed "the said coprocessor" to --said coprocessor-- (claims 6, 7, 13, 14 and 20), and changed "a logic circuit" to --a first logic circuit-- (claim 8).

Accordingly, Applicant solicits withdrawal of the objection to claims 5-7, 8, 12-14 and 20.

Claims 1-4, 6, 8-11, 13 and 15-20 have been rejected under 35 U.S.C. §102(e) as being anticipated by Freerksen et al.

The Examiner asserted that Freerksen et al. discloses an apparatus and method to improve performance of reads from and writes to shared memory locations identically corresponding to what is claimed. This rejection is respectfully traversed.

In more detail, as to the rejection for independent claim 1, the Examiner asserted that "Freerksen's synchronous signal producing circuit detects and prevents the coprocessor from accessing stale data from shared memory [by] putting the processor in a wait/retry state, thus an inhibit region register, a comparison circuit and a first logic circuit are required in order to carry out the specified tasks," citing column 8, lines 3-26 from Freerksen et al. The following is reproduction of part of the Examiner's cited portion.

> To prevent processor 110 from retrieving the old version of data from main memory, bus controller 128, which snoops bus 150 (in particular, the command bus in system bus 150) and sees the read, broadcasts a retry transaction on the response bus. Processor 110 then stops its read and waits a time to retry the read. See column 8, lines 3-26.

It is Applicant's understanding that a basic concept of the Feerkson system is to give a writing operation to a shared memory location priority over a reading operation from the shared memory location, once the writing operation to the shared memory location has been rejected at least once (column 3, lines 18-25).

The Examiner did not discharge his burden.

In denying patentability to a claimed invention based upon prior art, the Examiner must point to "page and line" of a reference wherein each feature of a claimed invention is asserted to reside. *In re Rijckaert*, 9 F.3d 1531, 28 USPQ2d 1955 (Fed. Cir. 1993). Indeed, the Examiner must not only point to "column and line of each relevant prior art reference," but must also explain how one having ordinary skill in the art would have interpreted each of the relied upon

portions of the cited references. *Ex parte Gambogi*, 62 USPQ2d 2019 (BPAI 2001). That burden has not been discharged.

In this Office Action, the Examiner merely cited one paragraph (see above) and concluded that "an inhibit region register, a comparison circuit and a first logic circuit are required [in the Freerksen system] in order to carry out the specified tasks" (page 4, lines 9-11 of the Office Action).

In response, Applicant submits that the Examiner did not show any factual basis for reaching such a conclusion, and did not identify what in Freerksen et al. correspond to the claimed elements. The Examiner's assertion "Freerksen's synchronous signal producing circuit detects and prevents the coprocessor from accessing stale data from shared memory [by] putting the processor in a wait/retry state" does not suggest any specific hardware structure as recited in claim 1. It is believed that a specific hardware structure of the claimed invention cannot straightforwardly be obtained from Freerksen et al. based only on such an abstract function asserted by the Examiner without identifying any corresponding elements in Freerksen et al. Again, the Examiner is required to identify where the reference shows each element of the claimed invention.

The claimed invention is not disclosed by Freerksen et al.

The factual determination of lack of novelty under 35 U.S.C. §102 requires the identical disclosure in a single reference of each element of the claimed invention, such that the identically claimed invention is placed into the possession of one having ordinary skill in the art. *Helifix Ltd. v. Blok-Lok, Ltd.*, 208 F. 3d 1339, 54 USPQ2d 1299 (Fed. Cir. 2000); *Electro Medical Systems S.A. v. Cooper Life Sciences, Inc.*, 34 F.3d 1048, 32 USPQ2d 1017 (Fed. Cir. 1994).

Based on the above legal tenet, Applicant submits that Freerksen et al. does not explicitly or implicitly disclose a synchronous signal producing circuit including an access inhibit region register, a comparing circuit and a first logic circuit, recited in claim 1, within the meaning of 35 U.S.C. §102.

As mentioned above, Freerksen et al. merely discloses that "bus controller 128, ... snoops bus 150 (in particular, the command bus in system bus 150) and sees the read, broadcasts a retry transaction on the response bus," and "Processor 110 then stops its read and waits a time to retry the read." (see column 8, lines 3-26). It is thus apparent that Freerksen et al. does not disclose anything about an "access inhibit region register," "comparing circuit" and "first logic circuit," as recited in claim 1. In other words, Freerksen et al. does not provide the identical disclosure of each element of the claimed invention. *Helifix Ltd.*, 208 F. 3d 1339; *Electro Medical Systems S.A.*, 34 F.3d 1048.

The above-described fundamental deficiencies of the Examiner's rejection and the disclosure of Freerksen et al. undermine the factual determination that Freerksen et al. identically describes the claimed invention within the meaning 35 U.S.C. §102. Applicant, therefore, submits that the imposed rejection of claim 1 under 35 U.S.C. §102(e) for lack of novelty as evidenced by Freerksen et al. is not factually viable and, hence, respectfully solicits withdrawal thereof.

Applicant also notes that the above discussion can be applied to other independent claims 8 and 15 (see the Examiner's comments at page 6, the first and second full paragraphs of the Office Action), and thus the limitations recited in claims 8 and 15 are not disclosed by Freerksen et al. Therefore, withdrawal of the rejection of claims 8 and 15 is respectfully solicited.

Applicant further note that a dependent claim is not anticipated if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claim. Therefore, claims 2-4, 5, 9-11, 13 and 16-20 are patentable because they respectively include all the limitations of independent claims 1, 8 and 15. The Examiner's additional comments with respect to claims 2-4, 5, 9-11, 13 and 16-20 do not cure the argued fundamental deficiencies of Freerksen et al. Accordingly, Applicants respectfully traverses the rejections of those claims and solicits withdrawal thereof.

Claims 5 and 12 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Freerksen et al. in view of Yamada.

In the statement of the rejection, the Examiner admitted that Freerksen et al. fails to teach a logic circuit for issuing a signal setting a processor to a low power consumption mode. Then, the Examiner asserted that the secondary reference, Yamada, teaches such a missing feature and concluded that it would have been obvious to modify Freerksen's apparatus based on the teachings of Yamada. Applicant respectfully traverses this rejection.

Applicant submits that the Examiner has not established a *prima facie* basis to deny patentability to the claimed invention under 35 U.S.C. §103 for lack of the requisite factual basis. To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). The proposed combination of Freerksen et al. and Yamada does not teach or suggest each and every limitation of claims 5 and 12.

Applicant understands that Yamada discloses "a second instruction decoder receiving at least a portion of the instruction applied from the instruction register to the first instruction decoder so as to supply a standby control signal to the execution unit" (column 3, lines 21-24).

However, Yamada does not teach all the limitations recited in claims 5 and 12. The reference does not teach that a low consumption mode signal is issued "based on the signal indicating that said coprocessor is executing the coprocessor instruction as well as the result of the comparison by said comprising circuit." As discussed above, Freerksen et al. does not disclose at least the comparison circuit of the claimed invention, either.

Based upon the forgoing, the proposed combination of Freerksen et al. and Yamada does not disclose all the limitations recited in claims 5 and 12, even if the reference teachings were to be combined. Accordingly, in the instant case, the pending rejection has not established *prima facie* obviousness of the claimed invention as recited in claims 5 and 12, because the proposed combination fails to satisfy the requirement under 35 U.S.C. §103 that all the claim limitations must be taught or suggested by the prior art. *See In re Royka*, 490 F.2d 981. Applicant, therefore, solicits withdrawal of the rejection of claims 5 and 12.

Conclusion.

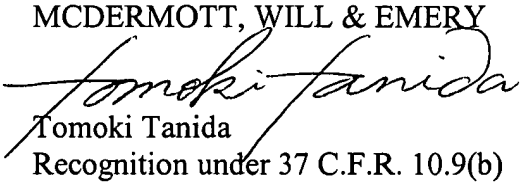
Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, Examiner is requested to call Applicant's attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper,

including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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